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Applicant:	Larry D. Hewitt and Dale E. Gulick		
Title:	CONFIGURING A COMMUNICATION LINK INTERFACE		
Application No.:	10/647,397	Filed:	August 25, 2003
Examiner:	King, Justin	Group Art Unit:	2111
Atty. Docket No.:	1001-0021-1	Conf. No.:	3675

Dear Sir:

Transmitted herewith are the following document(s) in the above-identified application:

(1) This Transmittal Letter (1 page(s))
(2) Appeal Brief (37 C.F.R. § 41.37) (25 page(s))

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Michael R. Long 03-24-06
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Title:	CONFIGURING A COMMUNICATION LINK INTERFACE		
Application No.:	10/647,397	**Filed:**	August 25, 2003
Examiner:	King, Justin	**Group Art Unit:**	2111
Atty. Docket No.:	1001-0021-1	**Confirmation No.:**	3675

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(1) Appeal Brief (37 C.F.R. § 41.37) (25 pages)
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal, filed on January 25, 2006. The fee required under 37 C.F.R. § 41.20(b)(2) is provided in the accompanying Transmittal.

REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc., the assignee of record, as evidenced by the assignment recorded at Reel/Frame 010250/0736.

RELATED APPEALS AND INTERFERENCES

Known prior and pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal include:

None.

STATUS OF CLAIMS

Claims 1, 8-17, 19 and 20 are pending. Claims 1, 8-17, 19 and 20 stand as rejected. Rejected claims 1, 8-17, 19 and 20 are the subject of this appeal.

STATUS OF AMENDMENTS

The amendment filed on March 3, 2006, canceling claims 2-7 and 18 and amending independent claim 1 to include the subject matter of dependent claim 18 has been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a method 3200 (see Fig. 32) of configuring a communication link interface (e.g., side A link interface 305 of Fig. 4). The method 3200 comprises: setting a transmit width of a transmit portion of the link interface 305 based on a usable transmit width 3206; and setting a receive width of a receive portion of the link interface 305 based on a usable receive width 3208 (see Appellants' specification at the new paragraph following paragraph 1268). The transmit and receive widths are separately specified. As is set forth in Appellants' specification, a receive controller 413 and a transmit controller 415 may further include a link bridge register 3101 or 3102 (see Fig. 31) that is programmable and may include four separate fields that allow for setting a receive width, a maximum receive width, a transmit width and a maximum transmit width (see Appellants' specification at page 64, paragraph 1266). With reference to Appellants' specification, beginning at page 64 (paragraph 1266) through page 70 (paragraph 1293), a table depicts upstream and downstream link width registers as including four separate fields, i.e., a receive width field, a receive maximum width field, a transmit width field and a transmit maximum width field.

Independent claim 8 is directed to a communication link interface (e.g., side A link interface 305 of Fig. 4) comprising: a transmit controller (e.g., transmit controller 415 of Fig. 4) to transmit data over a transmit portion of the link interface 305 and a receive controller (e.g., receive controller 413 of Fig. 4) to receive data over a receive portion of the link interface 305. A width of data transmitted is set according to a value held in a programmable transmit width register and a width of data received is set according to a value held in a programmable receive width register. As noted above, the link interface 305 may further include a link bridge register 3101 or 3102 (see Fig. 31) that is programmable and may include four separate fields that allow for setting a receive width, a maximum receive width, a transmit width and a maximum transmit width. With reference to Appellants' specification, beginning at page 64 (paragraph 1266) through page 70 (paragraph 1293), a table depicts upstream and downstream link width registers

as including four separate fields, i.e., a receive width field, a receive maximum width field, a transmit width field and a transmit maximum width field.

Claim 12, which depends upon claim 8, includes the additional limitations that the communication link interface has a maximum transmit width register indicating a physical width of a transmit portion of the link interface and a maximum receive width register indicating a physical width of a receive portion of the link interface. As noted above, the receive controller 413 and the transmit controller 415 (see Fig. 4) may further include a link bridge register 3101 or 3102 (see Fig. 31) that is programmable and may include four separate fields that allow for setting a receive width, a maximum receive width, a transmit width and a maximum transmit width (see Appellants' specification at page 64, paragraph 1266).

Claim 19, which depends upon claim 8, includes the additional explicit limitation that the width of the data transmitted and the width of the data received are separately specified. As noted above, the receive controller 413 and the transmit controller 415 may further include a link bridge register 3101 or 3102 (see Fig. 31) that is programmable and may include four separate fields that allow for setting a receive width, a maximum receive width, a transmit width and a maximum transmit width (see Appellants' specification at page 64, paragraph 1266).

Independent claim 13 is directed to a communication link interface comprising a means for setting a transmit width of a transmit portion of the link interface, based on a usable transmit width, and a means for setting a receive width of a receive portion of the link interface, based on a usable receive width. As is set forth in paragraph 1267 of Appellants' specification, in one embodiment a BIOS is utilized to program a width field of a transmit controller on side A of a link to match a width field of a receive controller on side B of the link. As is set forth in Appellants' specification, a receive controller 413 and a transmit controller 415 (see Fig. 4) may further include a link bridge register 3101 or 3102 (see Fig. 31) that is programmable and may include four separate fields that allow for setting a receive width, a maximum receive width, a transmit width and a maximum transmit width (see Appellants' specification at page 64, paragraph 1266). In general, the width fields may be programmed to be the lesser of the maximum width values on the two sides. In this embodiment, the BIOS may also program a width field of a transmit controller on side B of the link to match a width field of a receive

controller on side A of the link in a similar fashion. In this manner, integrated circuits (ICs) can implement different size data buses for the transmit and receive controllers and still be able to communicate with other IC links having different size data buses.

Claim 16, which depends upon independent claim 13, includes the additional limitations that the communication link interface includes a means for providing a maximum transmit width for use in determining a usable transmit width and a means for providing a maximum receive width for use in determining a usable receive width. As is set forth in Appellants' specification, a receive controller 413 and a transmit controller 415 (see Fig. 4) may further include a link bridge register 3101 or 3102 (see Fig. 31) that is programmable and may include four separate fields that allow for setting a receive width, a maximum receive width, a transmit width and a maximum transmit width (see Appellants' specification at page 64, paragraph 1266). With reference to Appellants' specification, beginning at page 64 (paragraph 1266) through page 70 (paragraph 1293), a table depicts upstream and downstream link width registers as including four separate fields, i.e., a receive width field, a receive maximum width field, a transmit width field and a transmit maximum width field.

Claim 17, which depends upon independent claim 13, includes the additional limitations that the communication link interface includes a means for providing a maximum transmit width for use in determining a usable receive width of another communication link interface and a means for providing a maximum receive width for use in determining a usable transmit width of another communication link interface. As is set forth in Appellants' specification, a receive controller 413 and a transmit controller 415 (see Fig. 4) may further include a link bridge register 3101 or 3102 (see Fig. 31) that is programmable and may include four separate fields that allow for setting a receive width, a maximum receive width, a transmit width and a maximum transmit width (see Appellants' specification at page 64, paragraph 1266). With reference to Appellants' specification, beginning at page 64 (paragraph 1266) through page 70 (paragraph 1293), a table depicts upstream and downstream link width registers as including four separate fields, i.e., a receive width field, a receive maximum width field, a transmit width field and a transmit maximum width field.

Claim 20, which depends upon claim 13, includes the additional explicit limitation that the transmit and receive widths of the interface are separately specified. As noted above, a receive controller 413 and a transmit controller 415 may further include a link bridge register 3101 or 3102 (see Fig. 31) that is programmable and may include four separate fields that allow for setting a receive width, a maximum receive width, a transmit width and a maximum transmit width (see Appellants' specification at page 64, paragraph 1266).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Ground I: The rejection of claims 1, 8-17, 19 and 20, under 35 U.S.C. §102(b), as being anticipated by U.S. Patent No. 5,812,798, issued to Moyer et al.

Ground II: The rejection of claims 1, 8-17, 19 and 20, under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent No. 5,255,374, issued to Aldereguia et al., in view of U.S. Patent No. 5,812,798, issued to Moyer et al.

Argument

In the arguments below, brief descriptions are provided for each of the applied references, followed by Appellants' arguments as to why claims 1, 8-17, 19 and 20 are not anticipated, under 35 U.S.C. §102(b), by U.S. Patent No. 5,812,798, issued to Moyer et al., and why a *prima facie* case of obviousness, under 35 U.S.C. § 103(a), has not been established based upon U.S. Patent No. 5,255,374, issued to Aldereguia et al., in view of U.S. Patent No. 5,812,798, issued to Moyer et al.

U.S. Patent No. 5,812,798

U.S. Patent No. 5,812,798 issued to Moyer et al. (hereinafter "Moyer") is directed to a data processing system 15 that includes a data processor 10 that may interface with a variety of devices 51, 52, 53, 54, 56, 58 and 72, e.g., memory devices and external peripheral devices (see Fig. 1), at least some of which have different bus widths. The processor 10 includes a central processing unit (CPU) 12 and a system integration unit (SIU) 22. The SIU 22 includes control

registers 94 that may be read by or written to by the CPU 12 (see Fig. 2). The control registers 94 include a plurality of peripheral control registers 95 (see Fig. 3) and a chip select control register, which includes bus loading control bits, address range bits and other chip select control bits. In the data processing system 15, each of the devices 51-54, 56, 58 and 72 is assigned an address range in a memory map of the data processor 10. A set of data port size (DSZ) bits, located in the control register 94, define a data bit width of a device data port, as well as a plurality of integrated circuit terminals, which comprise the device data port. To configure the plurality of integrated circuit terminals, bus coupling circuitry 100 (see Fig. 2) evaluates the DSZ bits (value) and selectively enables a portion of the plurality of integrated circuit terminals in response thereto. The DSZ values are programmed into the registers 94 during initialization of the data processor 10. As is noted at col. 13, lines 23-25, the DSZ values must be carefully programmed to correctly implement a circuit board configuration of the data processing system 15.

By programming the DSZ value stored in one of the plurality of control registers 94, the user may configure the data processor 10 to communicate either eight, sixteen, or thirty-two bit data, via an appropriate 8-bit byte lane or plurality of 8-bit byte lanes, depending on the device accessed. In this manner, a user may balance loading on each of the plurality of integrated circuit terminals, such that power consumption and timing may be optimized. As is disclosed, because the data transferred on each of the plurality of integrated circuit terminals is balanced, the average power consumed by the data processing system 15 is lowered (as compared to prior art systems) and the capacitance associated with over-loading is distributed.

In a disclosed embodiment, if the DSZ bits have a binary value of: %000, the data processor 10 is configured to communicate data via an eight bit port which resides on a plurality of integrated circuit terminals that provides data bits D31 through D24 to bus 60; %001, the data processor 10 is configured to communicate data via an eight bit port which resides on a plurality of integrated circuit terminals that provides data bits D23 through D16 to bus 60; %010, the data processor 10 is configured to communicate data via an eight bit port which resides on a plurality of integrated circuit terminals that provides data bits D15 through D8 to bus 60; %011, the data processor 10 is configured to communicate data via an eight bit port which resides on a plurality of integrated circuit terminals that provides data bits D7 through D0 to bus 60.

In a disclosed embodiment, for data values having a bit width of sixteen bits, the data may be transmitted and received by the data processor 10 using one of two pluralities of integrated circuit terminals. If the DSZ bits have a binary value of: %100, the data processor 10 is configured to communicate data via a sixteen bit port which resides on a plurality of integrated circuit terminals that provides data bits D31 through D16 to bus 60. If the DSZ bits have a binary value of %101, the data processor 10 is configured to communicate data via a sixteen bit port which resides on a plurality of integrated circuit terminals that provides data bits D15 through D0 to bus 60. In a disclosed embodiment, when the data processor 10 receives a data value having a data bit width of thirty-two, the DSZ bits are set to %110 and the data processor 10 is configured to communicate all thirty-two bits of data on a plurality of integrated circuit terminals designated for receiving data bits D31 through D0.

U.S. Patent No. 5,255,374

U.S. Patent No. 5,255,374 issued to Aldereguia et al. (hereinafter "Aldereguia") is directed to a bus interface unit (BIU) 64 that includes translation logic 108 (see Fig. 2) for temporarily storing, in response to a predetermined set of operating conditions, data transferred between a system bus and an I/O bus. The translation logic 108 allows data transferred between a faster system device to a slower I/O device to be temporarily stored. The translation logic also facilitates conversion of 32-bit read and write cycles, initiated on the system bus, to four 8-bit or two 16-bit cycles or single 16-bit read and write cycles, initiated on the system bus, to two 8-bit cycles.

Ground I: The rejection of claims 1, 8-17, 19 and 20 under 35 U.S.C. §102(b) as being anticipated by Moyer.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). As Moyer does not disclose, expressly or inherently, each and every element claimed in Appellants' independent claims, Moyer cannot anticipate Appellants' claims.

Claim 1

With specific reference to independent claim 1, Appellants submit that Moyer does not disclose setting a transmit width of a transmit portion of a link interface, based on a usable transmit width, and a receive width of a receive portion of the link interface, based on a usable receive width, wherein the transmit and receive widths are separately specified. The final Office Action, mailed October 25, 2006, at page 2, states "Moyer discloses the microprocessor adjusts the bit width (column 2, lines 12-21). Moyer discloses allocating the bus bit width and position in transmitting the data (column 3, lines 20-26). Moyer's microprocessor adjusting the bit width is equivalent to the claimed setting receive width; Moyer's allocating the bus bit width and position is equivalent to the claimed setting a transmit width." At the outset, Appellants note that the cited passage, at column 2, lines 12-21, is set forth in Moyer's background and is referring to operation of a prior art MC68020 microprocessor, which dynamically determines whether a data bit width is eight, sixteen or thirty-two bits, during each bus cycle. During a data transfer operation, an external device coupled to the MC68020 microprocessor signals a required data bit width. That signaled data bit width is then utilized for communication between the MC68020 microprocessor and the external device. Moreover, there is no indication that the MC68020 microprocessor utilizes other than a single data bit width for both transmitting data to and receiving data from a given external device. As specifically noted by Moyer, the operation of the MC68020 microprocessor may cause load imbalance on integrated circuit (IC) terminals of the MC68020 microprocessor, as some of the IC terminals are utilized more often than other IC terminals of the MC68020 microprocessor (see Moyer column 2, lines 26-46). Thus, Moyer seeks to address the load imbalance problem present in devices, such as the prior art MC68020 microprocessor.

However, as is noted above, at most Moyer discloses setting a single device data port width that is used for both transmitting and receiving data between a data processor and a given memory device or external peripheral device (see Moyer Fig. 1). That is, while Moyer does disclose allocating a bus width and position for data, the width for both transmission and receipt of the data between the Moyer data processor and another given device is the same. According to one of Appellants' disclosed embodiments, as is set forth in paragraph 1266 of Appellants' specification, upstream and downstream links include registers having four separate fields, i.e., a

receive width field, a receive maximum width field, a transmit width field and a transmit maximum width field. As is set forth in paragraph 1267 of Appellants' specification, in one embodiment a BIOS is utilized to program the width field of a transmit controller on side A of the link to match a width field of a receive controller on side B of the link. In general, the width fields may be programmed to be the lesser of the maximum width values on the two sides. In a disclosed embodiment, the BIOS may also program a width field of a transmit controller on side B of the link to match a width field of a receive controller on side A of the link. In this manner, integrated circuits (ICs) can implement different size data buses, for the transmit and receive controllers, and still be able to communicate with other ICs having different size data buses. In sum, while Moyer allows for defining a data bit width of a device data port, Moyer does not teach, nor does Moyer suggest, setting both a transmit width of a transmit portion of a link interface based on a usable transmit width and a receive width of a receive portion of the link interface based on a usable receive width.

The final Office Action in rejecting Appellants' dependent claims 18-20 states, at page 4, the following: "[r]eferring to claims 18-20: Since Moyer discloses that CPU sets the transmit width (column 2, lines 14-19), and Moyer discloses that the data port size (DSZ) is initialized (column 6, lines 30-32, column 13, lines 18-20). Hence, Moyer discloses transmit and receive widths are separately specified." While Appellants are unsure of the meaning of the above quoted passage, Appellants note that Moyer column 2, lines 14-19 refers to the prior art MC68020 microprocessor discussed above. Further, as noted above, while Moyer allows for defining a data bit width of a device data port, Moyer does not teach, nor does Moyer suggest, setting both a transmit width of a transmit portion of a link interface based on a usable transmit width and a receive width of a receive portion of the link interface based on a usable receive width. Moreover, Moyer's communication interface is incapable of separately specifying a receive width and a transmit width of a communication link interface, as is now explicitly set forth in Appellants' independent claim 1, as amended on March 3, 2006, to include the subject matter of dependent claim 18. Furthermore, a fair reading of Moyer's description of the MC68020 microprocessor would also lead to the conclusion that the MC68020 is also not capable of separately specifying a receive width and a transmit width of a communication link interface. For at least the above reasons, claim 1 is allowable over Moyer.

Claims 8-11

With specific reference to independent claim 8, Appellants submit that Moyer does not disclose a communication link interface that includes a transmit controller whose transmit data width is set according to a value held in a programmable transmit width register and a receive controller whose receive data width is set according to a value held in a programmable receive width register. At most, as is set forth above, Moyer discloses setting a single width register that is used to set both a transmit width and a receive width for a device data port. As noted above, paragraph 1266 of Appellants' specification, discloses an embodiment in which upstream and downstream links include registers having four separate fields, i.e., a receive width field, a receive maximum width field, a transmit width field and a transmit maximum width field. As is noted above, in one embodiment, a BIOS is utilized to program the width field of a transmit controller on side A of the link to match a width field of a receive controller on side B of the link. In this embodiment, the BIOS may also program a width field of a transmit controller on side B of the link to match a width field of a receive controller on side A of the link in a similar fashion. With specific reference to Appellants' Fig. 4, an exemplary communication link, including a data bus, a link interface side A and a link interface side B, is depicted.

While Moyer allows for defining a data bit width of a device data port, Moyer does not teach, nor does Moyer suggest, a communication link interface that includes separate programmable transmit and receive width registers. In sum, Moyer merely discloses programming a DSZ value stored in one of a plurality of control registers 94 to configure a data processor 10 to communicate either 8, 16 or 32 bit data, via an appropriate 8-bit byte lane or plurality of 8-bit byte lanes, depending upon an external device accessed (see Moyer column 12 lines 15-20). Furthermore, Moyer's communication interface is incapable of separately specifying a receive width and a transmit width of a communication link interface. Moreover, as noted above, a fair reading of Moyer's background discussion of the MC68020 microprocessor would lead one to conclude that the MC68020 microprocessor also utilizes a single data bit width for both transmitting data to and receiving data from a given external device. For at least the above reasons, independent claim 8 and dependent claims 9-11 are allowable over Moyer.

Claim 12

With reference to claim 12, which depends upon independent claim 8, Appellants submit that Moyer does not disclose a communication link interface having a maximum transmit width register indicating a physical width of a transmit portion of the link interface and a maximum receive width register indicating a physical width of a receive portion of the link interface. As noted above, at most Moyer discloses setting a single device data port width that is used for both transmitting and receiving data between a data processor and a given memory device or external peripheral device (see Moyer Fig. 1). That is, while Moyer does disclose allocating a bus width and position for data, the width for both transmission and receipt of the data between the Moyer data processor and another given device is the same and as noted above only teaches the use of a single register. For at least the above reasons, claim 12 is allowable over Moyer.

Claim 19

With reference to claim 19, which depends upon independent claim 8, as noted above, while Moyer allows for defining a data bit width of a device data port, Moyer does not teach, nor does Moyer suggest, setting both a width of data transmitted and a width of data received according to values held in programmable transmit and receive width registers, respectively. Moreover, Moyer's communication interface is incapable of separately specifying a receive width and a transmit width of a communication link interface, as is set forth in Appellants' dependent claim 19. For at least the above reasons, claim 19 is allowable over Moyer.

Claims 13-15

With reference to independent claim 13, Appellants submit that Moyer does not disclose means for setting both a transmit width of a transmit portion of a link interface and a receive width of a receive portion of the link interface, based upon usable transmit and receive widths, respectively. At most, as is set forth above, Moyer discloses setting a device data port width that is used for both transmitting and receiving data. As is set forth in paragraph 1266 of Appellants' specification, in one embodiment, upstream and downstream links include registers having four separate fields, i.e., a receive width field, a receive maximum width field, a transmit width field and a transmit maximum width field. As is set forth in paragraph 1267 of Appellants' specification, in one embodiment a BIOS is utilized to program the width field of a transmit

controller on side A of the link to match a width field of a receive controller on side B of the link. In general, the width fields are programmed to be the lesser of the maximum width values on the two sides. In this embodiment, the BIOS may also program a width field of a transmit controller on side B of the link to match a width field of a receive controller on side A of the link in a similar fashion. In this manner, integrated circuits can implement different size data buses for the transmit and receive controllers and still be able to communicate with other IC links having different size data buses.

While Moyer allows for defining a data bit width of a device data port, Moyer does not teach, nor does Moyer suggest, setting both a transmit width of a transmit portion of a communication link interface and a receive width of a receive portion of the link interface, based upon usable transmit and receive widths, respectively. In sum, as noted above, Moyer merely discloses programming a DSZ value stored in one of a plurality of control registers 94 to configure a data processor 10 to communicate either 8, 16 or 32 bit data, via an appropriate 8-bit byte lane or plurality of 8-bit byte lanes, depending upon an external device accessed (see Moyer column 12 lines 15-20). For at least the above reasons, independent claim 13 and dependent claims 14-15 are allowable over Moyer.

Claim 16

With reference to claim 16, which depends upon independent claim 13, Appellants submit that Moyer does not disclose a means for providing a maximum transmit width for use in determining a usable transmit width and a means for providing a maximum receive width for use in determining a usable receive width. As noted above, Moyer merely discloses programming a DSZ value stored in one of a plurality of control registers 94 to configure a data processor 10 to communicate either 8, 16 or 32 bit data, via an appropriate 8-bit byte lane or plurality of 8-bit byte lanes, depending upon an external device accessed (see Moyer column 12 lines 15-20). For at least the above reasons, claim 16 is allowable over Moyer.

Claim 17

With reference to claim 17, which depends upon independent claim 13, Appellants submit that Moyer does not disclose a means for providing a maximum transmit width for use in determining a usable receive width of another communication link interface and a means for

providing a maximum receive width for use in determining a usable transmit width of another communication link interface. As noted above, Moyer merely discloses programming a DSZ value stored in one of a plurality of control registers 94 to configure a data processor 10 to communicate either 8, 16 or 32 bit data, via an appropriate 8-bit byte lane or plurality of 8-bit byte lanes, depending upon an external device accessed (see Moyer column 12 lines 15-20). For at least the above reasons, claim 17 is allowable over Moyer.

Claim 20

With reference to claim 20, which depends upon independent claim 13, as noted above, while Moyer allows for defining a data bit width of a device data port, Moyer does not teach, nor does Moyer suggest, setting both a transmit width of a transmit portion of a link interface based on a usable transmit width and a receive width of a receive portion of the link interface based on a usable receive width. Moreover, Moyer's communication interface is incapable of separately specifying a receive width and a transmit width of a communication link interface, as is set forth in Appellants' dependent claim 20. For at least the above reasons, claim 20 is allowable over Moyer.

Ground II: The rejection of claims 1, 8-17, 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over the combination of Aldereguia and Moyer.

Appellants respectfully submit that the Examiner has failed to establish *prima facie* obviousness of the claimed invention recited in claims 1, 8-17, 19 and 20 over the teaching of Aldereguia in combination with Moyer. As a general proposition, obviousness is a legal determination based on underlying factual inquiries. *See* Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopedics, Inc., 976 F.2d 1559, 24 U.S.P.Q.2d (BNA) 1321, 1332-1333 (Fed. Cir. 1992). Graham v. John Deere Co., 383 U.S. 1, 17 (1966) defines the factual inquiries utilized to evaluate the prior art. Specifically, the prior art is evaluated in terms of: (1) its scope and content; (2) the differences between the prior art and the claimed invention; (3) the level of ordinary skill in the art at the time the application was filed; and (4) objective, or secondary, evidence of nonobviousness such as commercial success, failure of others, long-felt need and unexpected results, which must be considered in reaching a conclusion of obviousness. Graham v. John Deere Co., 383 U.S. 1, 17, 148 U.S.P.Q. 459, 460 (1966); Panduit Corp. v. Dennison

Mfg. Co., 810 F.2d 1561, 1566-67, 1 U.S.P.Q.2d 1593, 1595-96 (Fed. Cir. 1987); Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 24 U.S.P.Q.2d 1321, 1333 (Fed. Cir. 1992).

"To reject claims in an application under section 103, an examiner must show an unrebutted *prima facie* case of obviousness." In re Rouffet, 149 F.3d 1350, 47 U.S.P.Q.2d (BNA) 1453 (Fed. Cir 1998). It must be shown that all limitations of the claims are taught or suggested by the references as combined or modified to establish this *prima facie* case of obviousness. *See* In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). The combination or modification of references for an obviousness rejection must be supported with "a showing of a suggestion or motivation to modify the teachings." In re Kotzab, 217 F.3d 1365, 55 U.S.P.Q.2d 1313 (Fed. Cir 2000). "The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases, the nature of the problem to be solved." In re Kotzab, 217 F.3d 1365, 55 U.S.P.Q.2d 1313 (Fed. Cir 2000), *citing* In re Dembiczak, 175 F.3d 994 at 999, 50 U.S.P.Q.2d 1614 at 1617 (Fed. Cir. 1999). Rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references is "the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis." In re Lee, 277 F.3d 1338, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002), *quoting* In re Dance, 160 F.3d 1339, 1343, 48 U.S.P.Q.2d 1635, 1637 (Fed. Cir. 1998).

Appellant submits that the cited combination does not teach or suggest all of the claimed features of the invention and, for at least this reason, Appellants submit that the Examiner has failed to establish a *prima facie* case of obviousness. Moreover, Appellants submit that Aldereguia adds nothing to Moyer of relevance to Appellants' claimed subject matter. As noted above, Aldereguia is merely directly to a bus interface unit (BIU) that includes translation logic (buffers) for temporarily storing, in response to a predetermined set of operating conditions, data transferred between a system bus and an I/O bus through the BIU. In pertinent part, the translation logic facilitates conversion of 32-bit read and write cycles to four 8-bit or two 16-bit cycles or 16-bit read and write cycles to two 8-bit cycles. As is set forth in further detail below, neither Aldereguia or Moyer, alone or in combination, teach or suggest setting both a transmit width of a transmit portion of a link interface and a receive width of a receive portion of the link

interface, based upon usable transmit and receive widths, respectively, or based upon values held in programmable transmit and receive width registers, respectively.

Claim 1

In addressing Aldereguia, the final Office Action stated, at page 5, "[s]ince the bridge connects to different I/O devices with different bus width, each data transmission between the bridge and a particular I/O device is set to the bus width according to that particular I/O device's data width, which is equivalent to the claimed setting a receive width." Appellants note, whether the Aldereguia memory controller 58 is reading from or writing to a given one of I/O devices 28, a data width communicated between bus interface unit 64 and a given one of the I/O devices 28 would have the same data width.

With specific reference to independent claim 1, Appellants submit that neither Moyer or Aldereguia, alone or in combination, teach or suggest setting a transmit width of a transmit portion of a link interface, based on a usable transmit width, and a receive width of a receive portion of the link interface, based on a usable receive width. At most, as is set forth above, Moyer discloses setting a single device data port width that is used for both transmitting and receiving data for each separate device with which the Moyer processor communicates. Similarly, Aldereguia merely discloses communicating data between a given I/O device and a bus interface unit, based on a single data width. In sum, while Moyer allows for defining a data bit width of a device data port, neither Aldereguia or Moyer, alone or in combination, teach or suggest, setting both a transmit width of a transmit portion of a link interface and a receive width of a receive portion of the link interface, based upon usable transmit and receive widths, respectively. Any assertion to the contrary appears to be based on impermissible hindsight in view of Appellants' own disclosure.

While Moyer allows for defining a data bit width of a device data port, neither Moyer or Aldereguia, alone or in combination, teach or suggest setting both a transmit width of a transmit portion of a link interface and a receive width of a receive portion of the link interface based upon usable transmit and receive widths, respectively, wherein the transmit and receive widths are separately specified. Moreover, both Aldereguia's and Moyer's communication interfaces are incapable of separately specifying a receive width and a transmit width of a communication

link interface, as is now explicitly set forth in Appellants' independent claim 1, as amended on March 3, 2006. For at least the above reasons, claim 1 is allowable over the combination of Aldereguia and Moyer.

Claims 8-11

With specific reference to independent claim 8, Appellants submit that neither Moyer or Aldereguia, alone or in combination, teach or suggest a communication link interface that includes a transmit controller, whose transmit data width is set according to a value held in a programmable transmit width register, and a receive controller, whose receive data width is set according to a value held in a programmable receive width register. At most, Moyer discloses setting a single width register that is used to set both a transmit width and a receive width for a device data port and Aldereguia adds nothing of relevance to Moyer, with respect to Appellants' claimed subject matter. In sum, both Aldereguia's and Moyer's communication interfaces are incapable of separately specifying a receive width and a transmit width of a communication link. For at least the above reasons, claims 8-11 are allowable over the combination of Aldereguia and Moyer.

Claim 12

With specific reference to claim 12, which depends upon independent claim 8, Appellants submit that neither Moyer or Aldereguia, alone or in combination, teach or suggest a communication link interface having a maximum transmit width register, indicating a physical width of a transmit portion of the link interface, and a maximum receive width register, indicating a physical width of a receive portion of the link interface. At most, as is set forth above, Moyer discloses setting a single width register that is used to set both a transmit width and a receive width for a device data port and Aldereguia adds nothing of relevance to Moyer, with respect to Appellants' claimed subject matter. For at least the above reasons, claim 12 is allowable over the combination of Aldereguia and Moyer.

Dependent Claim 19

With specific reference to claim 19, which depends upon independent claim 8, as noted above, while Moyer allows for defining a data bit width of a device data port, neither Moyer or

Aldereguia teach or suggest, alone or in combination, a communication link interface having a maximum transmit width register, indicating a physical width of a transmit portion of the link interface, and a maximum receive width register, indicating a physical width of a receive portion of the link interface. Furthermore, neither Moyer or Aldereguia disclose a communication link interface that is capable of separately specifying a receive width and a transmit width of a communication link interface, as is explicitly set forth in Appellants' dependent claim 19. For at least the above reasons, claim 19 is allowable over the combination of Aldereguia and Moyer.

Claims 13-15

With reference to independent claim 13, Appellants submit that neither Moyer or Aldereguia teach or suggest a means for setting both a transmit width of a transmit portion of a communication link interface and a receive width of a receive portion of the link interface, based upon usable transmit and receive widths, respectively. At most, as is set forth above, Moyer discloses setting a device data port width that is used for both transmitting and receiving data in a communication with any given device. As is set forth in paragraph 1266 of Appellants' specification, in one embodiment, upstream and downstream links include registers having four separate fields, i.e., a receive width field, a receive maximum width field, a transmit width field and a transmit maximum width field. As is set forth in paragraph 1267 of Appellants' specification, in one embodiment a BIOS is utilized to program the width field of a transmit controller on side A of the link to match a width field of a receive controller on side B of the link. In general, the width fields are programmed to be the lesser of the maximum width values on the two sides. In this embodiment, the BIOS may also program a width field of a transmit controller on side B of the link to match a width field of a receive controller on side A of the link in a similar fashion. As noted above, in this manner, integrated circuits can implement different size data buses for the transmit and receive controllers and still be able to communicate with other IC links having different size data buses.

As previously noted, while Moyer allows for defining a data bit width of a device data port, Moyer does not teach, nor does Moyer suggest, setting both a transmit width of a transmit portion of a communication link interface and a receive width of a receive portion of the link interface. In sum, Moyer merely discloses programming a DSZ value stored in one of a plurality of control registers 94 to configure a data processor 10 to communicate either 8, 16 or 32 bit

data, via an appropriate 8-bit byte lane or plurality of 8-bit byte lanes, depending upon an external device accessed (see Moyer column 12 lines 15-20). Furthermore, both Aldereguia's and Moyer's communication interfaces are incapable of separately specifying a receive width and a transmit width of a communication link. For at least the above reasons, claims 13-15 are allowable over the combination of Aldereguia and Moyer.

Claim 16

With reference to claim 16, which depends upon independent claim 13, Appellants submit that neither Aldereguia or Moyer, alone or in combination, teach or suggest a means for providing a maximum transmit width for use in determining a usable transmit width and a means for providing a maximum receive width for use in determining a usable receive width. As noted above, Moyer merely discloses programming a DSZ value stored in one of a plurality of control registers 94 to configure a data processor 10 to communicate either 8, 16 or 32 bit data, via an appropriate 8-bit byte lane or plurality of 8-bit byte lanes, depending upon an external device accessed (see Moyer column 12 lines 15-20) and Aldereguia adds nothing of relevance to Moyer. For at least the above reasons, claim 16 is allowable over the combination of Aldereguia and Moyer.

Claim 17

With reference to claim 17, which depends upon independent claim 13, Appellants submit that neither Aldereguia or Moyer, alone or in combination, teach or suggest a means for providing a maximum transmit width for use in determining a usable receive width of another communication link interface and a means for providing a maximum receive width for use in determining a usable transmit width of another communication link interface. As noted above, Moyer merely discloses programming a DSZ value stored in one of a plurality of control registers 94 to configure a data processor 10 to communicate either 8, 16 or 32 bit data, via an appropriate 8-bit byte lane or plurality of 8-bit byte lanes, depending upon an external device accessed (see Moyer column 12 lines 15-20) and Aldereguia adds nothing of relevance to Moyer. For at least the above reasons, claim 17 is allowable over the combination of Aldereguia and Moyer.

Claim 20

With reference to claim 20, which depends upon independent claim 13, as noted above, while Moyer allows for defining a data bit width of a device data port, neither Moyer or Aldereguia, alone or in combination, teach or suggest, a means for setting both a transmit width of a transmit portion of a link interface and a receive width of a receive portion of the link interface. Moreover, neither Aldereguia's interface or Moyer's interface are capable of separately specifying a receive width and a transmit width of a communication link, as is explicitly set forth in claim 20. For at least the above reasons, claim 20 is allowable over the combination of Aldereguia and Moyer.

CONCLUSION

For the at least the foregoing reasons, and as apparent from examining the invention defined by claims 1, 8-17, 19 and 20, when properly considering the cited references these claims define patentable subject matter. Accordingly, this honorable Board is respectfully requested to reverse the rejections of claims 1, 8-17, 19 and 20, under §102(b) and §103(a), and to direct that the claims of the present application be issued.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

☐ deposited with the US Postal Service with sufficient postage as first class mail and addressed as shown above.

☒ facsimile transmitted to the US Patent and Trademark Office.

Michael R. Long — 03-24-06

Michael R. Long | Date

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Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously Presented) A method of configuring a communication link interface, the method comprising:

setting a transmit width of a transmit portion of the link interface based on a usable transmit width; and

setting a receive width of a receive portion of the link interface based on a usable receive width, wherein the transmit and receive widths are separately specified.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Original) A communication link interface comprising:

a transmit controller to transmit data over a transmit portion of the link interface, wherein a width of data transmitted is set according to a value held in a programmable transmit width register; and

a receive controller to receive data over a receive portion of the link interface, wherein a width of data received is set according to a value held in a programmable receive width register.

9. (Previously presented) The communication link interface as in claim 8, wherein:

the value held in the programmable transmit width register indicates a usable transmit width; and

the value held in the programmable receive width register indicates a usable receive width.

10. (Original) The communication link interface as in claim 9, wherein the usable transmit width is the lesser of a maximum transmit width of the transmit portion of the link interface and a maximum receive width of a receive portion of another communication link interface.

11. (Original) The communication link interface as in claim 9, wherein the usable receive width is the lesser of a maximum receive width of the receive portion of the link interface and a maximum transmit width of a transmit portion of another communication link interface.

12. (Original) The communication link interface as in claim 8, further comprising:

a maximum transmit width register indicating a physical width of the transmit portion of the link interface; and

a maximum receive width register indicating a physical width of the receive portion of the link interface.

13. (Original) A communication link interface comprising:

means for setting a transmit width of a transmit portion of the link interface based on a usable transmit width; and

means for setting a receive width of a receive portion of the link interface based on a usable receive width.

14. (Original) The communication link interface as in claim 13, wherein the usable transmit width is the lesser of a maximum transmit width of the transmit portion of the link interface and a maximum receive width of a receive portion of another communication link interface.

15. (Original) The communication link interface as in claim 13, wherein the usable receive width is the lesser of a maximum receive width of the receive portion of the link interface and a maximum transmit width of a transmit portion of another communication link interface.

16. (Original) The communication link interface as in claim 13, further comprising:

means for providing a maximum transmit width for use in determining the usable transmit width; and

means for providing a maximum receive width for use in determining the usable receive width.

17. (Previously presented) The communication link interface as in claim 13, further comprising:

means for providing a maximum transmit width for use in determining a usable receive width of another communication link interface; and

means for providing a maximum receive width for use in determining a usable transmit width of another communication link interface.

18. (Canceled)

19. (Previously presented) The interface as in claim 8, wherein the width of the data transmitted and the width of the data received are separately specified.

20. (Previously presented) The interface as in claim 13, wherein the transmit and receive widths are separately specified.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. § 1.130, 1.131, or 1.132 or any other evidence entered by the Examiner and relied upon by Appellant in the appeal.

RELATED APPEALS APPENDIX

There are no decisions rendered by a court or the Board in any proceeding identified above in the Related Appeals and Interferences section.